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EXAMINER	
PHAM, EMILY P	

ART UNIT	PAPER NUMBER
2838	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/585,151	BROX, MARTIN	
	Examiner	Art Unit	
	Emily Pham	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 August 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *10-14,17-26 and 28-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10-14,17-26 and 28-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 November 2009* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the Amendment filed on 8/02/2010.

Claim Objections

2. Claim 17 is objected to because of the following informalities: line 2 of claim 17 recites "the reference voltage"; it appears either it should be "a reference voltage". Appropriate correction is required.

3. Claim 17 is objected to because of the following informalities: lines 2 and 3 of claim 17 recite "the voltage regulation circuit device"; it appears either it should be "a voltage regulation circuit device" or claim 17 is dependent on claim 14. Appropriate correction is required.

4. Claim 18 is objected to because of the following informalities: lines 2 claim 18 recites "the reference voltage"; it appears either it should be "a reference voltage". Appropriate correction is required.

5. Claim 18 is objected to because of the following informalities: lines 2 and 3 of claim 18 recite "the voltage regulation system circuit device"; it appears either it should be "a voltage regulation system circuit device". Appropriate correction is required.

6. Claim 26 is objected to because of the following informalities: lines 2 and 3 of claim 26 recite "the voltage regulation circuit device"; it appears either it should be "a voltage regulation circuit device" or claim 26 is dependent on claim 25. Appropriate correction is required.

7. Claim 28 is objected to because of the following informalities: lines 2 and 3 of claim 28 recite "the voltage regulation circuit device"; it appears either it should be "a voltage regulation circuit device" or claim 28 is dependent on claim 25. Appropriate correction is required.

8. Claim 29 is objected to because of the following informalities: lines 2 and 3 of claim 29 recite "the voltage regulation system circuit device"; it appears either it should be "a voltage regulation system circuit device". Appropriate correction is required.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 10-14, 17-26, and 28-32 are rejected under 35 U.S.C. 102(b) as being anticipated by Morishita (US Publication 2002/0030538).

Regarding independent claim 10: Morishita (For example: see FIG 1, FIG 12, and FIG 13) discloses a voltage regulation system comprising:

an input of the voltage regulating system being presented with a first voltage (FIG 1: EXV);

an output of the voltage regulation system having the first voltage (FIG 1: EXV) changed into a second voltage (FIG 1: IntVcc), which is available to be tapped at the output;

a first device (FIG 1: SA) for generating an essentially constant voltage (FIG 1: Output

Voltage from SA) from the first voltage (FIG 1: EXV), or a voltage derived from it, to provide the essentially constant voltage (FIG 1: Output Voltage from SA) on a first line (FIG 1: first line from SA);

a further device (FIG 1: MA and 1) for generating a variable further voltage (FIG 1: Output Voltage from MA) from the first voltage (FIG 1: EXV) or a voltage derived from it to provide the variable further voltage (FIG 1: Output Voltage from MA) on a second line (FIG 1: second line from MA) directly connected to the first line (FIG 1: first line from SA), the variable further voltage (FIG 1: Output Voltage from MA) tracking the first voltage (FIG 1: EXV); and

a device (FIG 1: 2) for activating and/or deactivating the further device (FIG 1: MA and 1) to an activated and/or deactivated state.

Regarding claim 11: Morishita (For example: see FIG 1, FIG 12, and FIG 13) discloses the voltage regulation system of claim 10, wherein the further voltage generated by the further device (FIG 1: MA and 1) can be higher than the voltage generated by the first device (FIG 1: SA) (For example: see paragraphs [0013], [0017], [0018], [0070], [0073], [0079], [0087], [0094], [0108], [011]).

Regarding claim 12: Morishita (For example: see FIG 1, FIG 12, and FIG 13) discloses the voltage regulation system of claim 10, wherein the further voltage generated by the further device (FIG 1: MA and 1) is proportional to the first voltage (FIG 1: EXV) or the voltage derived

from it.

Regarding claim 13: Morishita (For example: see FIG 1, FIG 12, and FIG 13) discloses the voltage regulation system of claim 12, wherein the further device (FIG 1: MA and 1) comprises a voltage divider circuit (FIG 12: 10).

Regarding claim 14: Morishita (For example: see FIG 1, FIG 12, and FIG 13) discloses the voltage regulation system of claim 12, wherein the voltage generated by the first device (FIG 1: SA) or a voltage derived from it, and the further voltage generated by the further device (FIG 1: MA and 1), or a voltage derived from it, can be used for controlling a voltage regulation circuit device (FIG 1: 3).

Regarding claim 17: Morishita (For example: see FIG 1, FIG 12, and FIG 13) discloses the voltage regulation System of claim 12, wherein, in the activated state of the further device (FIG 1: MA and 1), the height of the level of the reference voltage (FIG 1: input voltage of 3) used for the voltage regulation circuit device (FIG 1: 3) is determined by whichever of the voltages generated by the first and further device (FIG 1: MA and 1), or the voltages derived from them, exhibits the higher level (For example: see paragraphs [0013], [0017], [0018], [0070], [0073], [0079], [0087], [0094], [0108], [011]).

Regarding claim 18: Morishita (For example: see FIG 1, FIG 12, and FIG 13) discloses the voltage regulation system of claim 12, wherein, in the deactivated state of the further device (FIG 1: MA and 1), the height of the level of the reference voltage (FIG 1: input voltage of 3) used for the voltage regulation system circuit device is determined by the voltage generated by the first device (FIG 1: SA) or the voltage derived from it.

Regarding independent claim 19: Morishita (For example: see FIG 1, FIG 12, and FIG 13) discloses a method for the regulation of voltage comprising:

changing a first voltage (FIG 1: EXV) into a second voltage (FIG 1: IntVcc), wherein the second voltage (FIG 1: IntVcc) exhibits a

lower voltage level than the first voltage (FIG 1: EXV);

generating an essentially constant voltage (FIG 1: Output Voltage from SA) from the first voltage (FIG 1: EXV), or a voltage derived from it, to provide the essentially constant voltage (FIG 1: Output Voltage from SA) on a first line (FIG 1: first line from SA);

generating a variable further voltage (FIG 1: Output Voltage from MA) from the first voltage (FIG 1: EXV) or a voltage derived from it, to provide the variable further voltage (FIG 1: Output Voltage from MA) on a second line (FIG 1: second line from MA) directly connected to the first line (FIG 1: first line from SA), the variable further voltage (FIG 1: Output Voltage from MA) tracking the first voltage (FIG 1: EXV), wherein the further voltage can be higher than the constant voltage (FIG 1: Output Voltage from SA) generated from the first voltage (FIG 1: EXV) or the voltage derived from it (For example: see paragraphs [0013], [0017], [0018], [0070], [0073], [0079], [0087], [0094], [0108], [011]); and changing the essentially constant voltage (FIG 1: Output Voltage from SA) to provide the second voltage (FIG 1: IntVcc) in a first state and changing the greater of the essentially constant voltage (FIG 1: Output Voltage from SA) and the variable further voltage (FIG 1: Output Voltage from MA) to provide the second voltage (FIG 1: IntVcc) in a second state.

Regarding claim 20: Morishita (For example: see FIG 1, FIG 12, and FIG 13) discloses the method of claim 19, further comprising generating the further voltage such that it is proportional to the first voltage (FIG 1: EXV) or the voltage derived from it.

Regarding independent claim 21: Morishita (For example: see FIG 1, FIG 12, and FIG 13) discloses a voltage regulation system comprising:

an input having a first voltage (FIG 1: EXV);

an output having a second voltage (FIG 1: IntVcc);

a first device (FIG 1: SA) for generating an essentially constant voltage (FIG 1: Output Voltage from SA) from the first voltage (FIG 1: EXV) to

provide the essentially constant voltage (FIG 1: Output Voltage from SA) on a first line (FIG 1: first line from SA); and

means for generating a tracking voltage from the first voltage (FIG 1: EXV) that tracks the first voltage (FIG 1: EXV),

a further device (FIG 1: MA and 1) for generating a variable further voltage (FIG 1: Output Voltage from MA) from the tracking

voltage to provide the variable further voltage (FIG 1: Output Voltage from MA) on a second line (FIG 1: second line from MA) directly connected to the first line (FIG 1: first line from SA); and

a device (FIG 1: 2) for activating and/or deactivating the further device (FIG 1: MA and 1) to an activated and/or deactivated state.

Regarding claim 22: Morishita (For example: see FIG 1, FIG 12, and FIG 13) discloses the voltage regulation system of claim 21, wherein the further voltage

generated can be higher than the voltage generated by the first device (FIG 1: SA) (For example: see paragraphs [0013], [0017], [0018], [0070], [0073], [0079], [0087], [0094], [0108], [011]).

Regarding claim 23: Morishita (For example: see FIG 1, FIG 12, and FIG 13) discloses the voltage regulation system of claim 21, wherein the further voltage generated is proportional to the first voltage (FIG 1: EXV).

Regarding claim 24: Morishita (For example: see FIG 1, FIG 12, and FIG 13) discloses the voltage regulation system of claim 21, further comprising a voltage divider circuit (FIG 12: 10).

Regarding claim 25: Morishita (For example: see FIG 1, FIG 12, and FIG 13) discloses the voltage regulation system of claim 21, wherein the voltage generated by the first device (FIG 1: SA) and the further voltage generated can be used for controlling a voltage regulation circuit device (FIG 1: 3).

Regarding claim 26: Morishita (For example: see FIG 1, FIG 12, and FIG 13) discloses the voltage regulation system of claim 21, wherein the voltage generated by the first device (FIG 1: SA) and the further voltage generated can be used as a reference voltage for the voltage regulation circuit device (FIG 1: 2).

Regarding claim 28: Morishita (For example: see FIG 1, FIG 12, and FIG 13) discloses the voltage regulation system of claim 21, wherein, in the activated state of the further device (FIG 1: MA and 1), the height of the level of the reference voltage (FIG 1: Voltage on line IVL) used for the voltage regulation circuit device (FIG 1: 3) is determined by whichever of the voltages generated by the first and further device (FIG

1: MA and 1) exhibits the higher level (For example: see paragraphs [0013], [0017], [0018], [0070], [0073], [0079], [0087], [0094], [0108], [011]).

Regarding claim 29: Morishita (For example: see FIG 1, FIG 12, and FIG 13) discloses the voltage regulation system of claim 21, wherein, in the deactivated state of the further device (FIG 1: MA and 1), the height of the level of the reference voltage (FIG 1: Voltage on line IVL) used for the voltage regulation system circuit device (FIG 1: 3) is determined by the voltage generated by the first device (FIG 1: SA) or the voltage derived from it.

Regarding claim 30: Morishita (For example: see FIG 1, FIG 12, and FIG 13) discloses the voltage regulation system of claim 10, wherein the device (FIG 1: 2) for activating and/or deactivating the further device (FIG 1: MA and 1) comprises a register (FIG 13: DRM).

Regarding claim 31: Morishita (For example: see FIG 1, FIG 12, and FIG 13) discloses the voltage regulation system of claim 21, wherein the device (FIG 1: 2) for activating and/or deactivating the further device (FIG 1: MA and 1) comprises a register (FIG 13: DRM).

Regarding independent claim 32: Morishita (For example: see FIG 1, FIG 12, and FIG 13) discloses a voltage regulation system comprising:
a first reference voltage generator (FIG 13: CCS) configured to generate an essentially constant voltage (FIG 1: Output Voltage from SA) from a first voltage (FIG 1: EXV);
a first buffer (FIG 1: SA) configured to buffer the essentially constant voltage (FIG 1: Output Voltage from SA) to provide a first reference voltage on a first line (FIG 1: first

line from SA);

a second reference voltage generator (FIG 13: CVC) configured to generate a tracking voltage from the first voltage (FIG 1: EXV) that tracks the first voltage (FIG 1: EXV); a second buffer (FIG 1: MA and 1) configured to buffer the tracking voltage to provide a second reference voltage (FIG 1: Output Voltage from MA) on a second line (FIG 1: second line from MA) directly connected to the first line (FIG 1: first line from SA); a device (FIG 1: 2) for activating and deactivating the second buffer (FIG 1: MA and 1) to an activated or deactivated state; and a voltage regulator (FIG 1: 3) configured to provide a second voltage (FIG 1: IntVcc) based on the first voltage (FIG 1: EXV), the first reference voltage (FIG 1: Output Voltage from SA), and the second reference voltage (FIG 1: Output Voltage from MA).

Response to Arguments

11. Applicant's arguments with respect to claims 10-14, 17-26, and 28-32 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emily Pham whose telephone number is (571)270-3046. The examiner can normally be reached on Mon-Thu (7:00AM - 6:00PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Monica Lewis can be reached on (571) 272 - 1838. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Monica Lewis/
Supervisory Patent Examiner, Art Unit 2838

October 09, 2010

/EP/
Examiner, Art Unit 2838